Offer #2024-08380

Hardware developer / FPGA

Contract type : Fixed-term contract

Level of qualifications required : Graduate degree or equivalent

Other valued qualifications : PhD

Fonction : Temporary scientific engineer

About the research centre or Inria department

Le centre Inria Rennes - Bretagne Atlantique est un des huit centres d'Inria et compte plus d'une trentaine d'équipes de recherche. Le centre Inria est un acteur majeur et reconnu dans le domaine des sciences numériques. Il est au cœur d'un riche écosystème de R&D et d'innovation : PME fortement innovantes, grands groupes industriels, pôles de compétitivité, acteurs de la recherche et de l'enseignement supérieur, laboratoires d'excellence, institut de recherche technologique.

Context

As part of the Arsene project (PEPR Cybersecurity), Inria Rennes is offering an engineer position (with or without a PhD) within the TARAN team, in collaboration with the High Security Laboratory (LHS) of Rennes and the PACAP team. The work will involve developing an FPGA demonstrator integrating the secure IPs developed within the project. This is a unique opportunity to work on a cutting-edge project in the field of computer security and the architecture of processors and embedded systems.

Host Team:
The project will take place within the TARAN team (formerly CAIRN) at the IRISA/INRIA laboratory. The TARAN team, which comprises more than 35 members from Inria, Univ Rennes, and ENS Rennes, has participated in numerous national and European R&D projects and has strong industrial partnerships (e.g., Safran, Thales, Nokia, Orange, STMicroelectronics, and various SMEs). TARAN has recognized expertise in several areas related to the project, such as computer architectures, embedded system design, fault tolerance, safety-critical systems, hardware accelerators, and computer arithmetic. In the context of hardware security, the team also works closely with DGA-MI and ANSSI.

Assignment

The main mission will be to develop an FPGA demonstrator (Xilinx), integrating the secure IPs from the project. The goal is to build a System-on-Chip around a custom NaxRiscV out-of-order execution core tailored for security. This SoC must be capable of running Linux.

The secondary mission will be to improve and evolve the open-source tools required for the development of this SoC.

The position is open for 3 years.

Main activities

- Design of the SoC IP from the adaptation of a collection of standalone IPs.
- Synthesis of the SoC and programming of the FPGA.
- Setting up the software environment (Linux) to test this SoC.
- Setting up experiments to test the security hardening present in the SoC.
- Writing technical documentation.
- Writing scientific papers based on the results obtained.

Skills

- Deep knowledge of processor and embedded system architectures
- Experience in hardware and software development (languages and methods)
- Experience in FPGA and/or ASIC development
- Good communication and team working skills
- Mastery of technical English (written and spoken)

Acquiring new skills:
As a new member of the TARAN team, you will be integrated into a research group with excellent prestige and deep knowledge of embedded systems. The TARAN research group can provide you with a more solid

understanding and knowledge of computer architectures and hardware design. For instance, the host team has high-quality papers published using RISC-V-based processors and dedicated hardware designs, subjects that you will be able to learn much more about and increase your background in this area.

Benefits package

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  - Prise en charge à 50 % des frais de transport en commun sur le trajet domicile-travail ou FMD.
  - Restauration subventionnée
  - Prise en charge partielle des frais de mutuelle
  - Possibilité de télétravail (à hauteur de 90 jours annuels) et d'aménagement du temps de travail

Remuneration

 rémunération mensuelle brute à partir de 2655 euros selon diplôme et expérience

General Information

- **Theme/Domain** : Architecture, Languages and Compilation
  Information system (BAP E)
- **Town/city** : Rennes
- **Inria Center** : Centre Inria de l'Université de Rennes
- **Starting date** : 2025-04-01
- **Duration of contract** : 3 years
- **Deadline to apply** : 2025-03-15

Contacts

- **Inria Team** : TARAN
- **Recruiter** :
  Sentieys Olivier / Olivier.Sentieys@irisa.fr

About Inria

Inria is the French national research institute dedicated to digital science and technology. It employs 2,600 people. Its 200 agile project teams, generally run jointly with academic partners, include more than 3,500 scientists and engineers working to meet the challenges of digital technology, often at the interface with other disciplines. The Institute also employs numerous talents in over forty different professions. 900 research support staff contribute to the preparation and development of scientific and entrepreneurial projects that have a worldwide impact.

The keys to success

To succeed in this position, you must have a solid knowledge of embedded systems architecture, experience in hardware development, and a good understanding of hardening methods. Experience in evaluating the security of systems and in writing technical documentation and scientific papers will also be an asset.

> **Warning** : you must enter your e-mail address in order to save your application to Inria. Applications must be submitted online on the Inria website. Processing of applications sent from other channels is not guaranteed.

Instruction to apply

Defence Security :
This position is likely to be situated in a restricted area (ZRR), as defined in Decree No. 2011-1425 relating to the protection of national scientific and technical potential (PPST).Authorisation to enter an area is granted by the director of the unit, following a favourable Ministerial decision, as defined in the decree of 3 July 2012 relating to the PPST. An unfavourable Ministerial decision in respect of a position situated in a ZRR would result in the cancellation of the appointment.

Recruitment Policy :
As part of its diversity policy, all Inria positions are accessible to people with disabilities.